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RAiO

RA8803/8822

Two Layers Character/Graphic LCD Controller Specification

Version 2.5

January 10, 2006

RAiO Technology Inc.

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Update History		
Version	**Date**	**Description**
1.0.	March 10, 2004	First Release(Preliminary Version)
1.1.	March 18, 2004	Update RA8822 Bonding Pad
1.2	April, 12, 2004	Add Chapter 7-11 Extension Mode for Display
1.3	May 3, 2004	Rearrange
2.0	January 20, 2005	1. Announce 5V to 3.3V Dc to DC Converter function. Pin name "TEST" change to "VDD5", "VDD" change to "VDD3". 2. Update Chapter 6-12. 3. Update Table 9-2.
2.1	March 11, 2005	1. Add Section 5-3 and Table 5-2 2. Update the description of REG [31] (DWBR)
2.2	April 22, 2005	1. Update Table 5-2 2. Update the description of REG [31h] (DWBR) 2. Update the description of REG [81h]
2.3	August 4, 2005	1. Update the description of Pin AVDD and AGND. 2. Modify the description of Register [D0h]. 3. Modify Section 6-12-1: Power Architecture and Figure 6-7.
2.5	January 10, 2006	1. Update REG [A0h] Interrupt Setup & Status Register (INTR) 2. Update REG [D0h] LCD Contrast Control Register (LCCR) 3. Update REG [81h] Frame Rate Polarity Change at Common_A Register (FRCA) 4. Update Table 5-2: Registers Setting for LCM Resolution 5. Add Section 8-5: Product Number

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1. General Description

The RA8803/RA8822 is a Dot-Matrix LCD controller which support both text and graphics mode. It built-in two Display RAM for two layers display, and an embedded 512Kbyte character ROM that consists of Chinese, English and ASCII fonts. In text mode, the RA8803/8822 support Chinese BIG5 code or GB code. The system (MPU) does not need take a lot of time to show the Chinese font in graphics mode.

The RA8803/8822 support 8080/6800 like MPU interface, and also provide 4-Bitor 8-Bit data bus. For LCD driver interface, it support the most of LCD Driver in the world. The RA8803 supports maximum resolution of LCD panel is 320x240 dots, and RA8822 is 240x160 dots. If use extension mode then the RA8803 support up to 640x240(320x480) dots resolution of Panel, and RA8822 support up to 480x160(240x320) dots. The embedded 10-Bit ADC and Analog Switch provide the 4-wires Touch Panel interface. The 5-Bit DAC provides the contrast control of the LCD panel. The RA8803/8822 also provide a 4x8 or 8x8 Key-Scan interface that reduces the loading of MPU. Except for 16x16 Chinese font size, RA8803/8822 also provides a great choice of different font sizes, such as 32x32, 48x48, or even 64x64. The embedded 512Byte SRAM allows user build their own characters or symbols for convenience.

The RA8803/8822 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.

2. Feature

- Support Text and Graphics Mode
- Support 2-Layers Display(AND, OR, NOR, XOR), Built-in Two 9.6K/4.8Kbyte Display Data RAM
- Dual Page Support Maximum 320x240(RA8803) Or 240x160(RA8822) Dots Panel
- Extension Mode RA8803: 640x240(320x480) RA8822: 480x160(240x320) Dots
- Support 4/8Bit of 6800/8080 MPU Interface
- Built-In 8x8 Key-Scan Circuit
- Support Horizontal and Vertical Scrolling
- Support 4/8Bit LCD Driver Interface
- Built-In 512KByte Font ROM,
  - _ RA8803/8822-T: 13,094 Traditional Chinese Fonts
  - _ RA8803/8822-S: 7,602 Simple Chinese Fonts
- Built-In 512Byte SRAM for Create Font
- Font Size Adjustable: 32x32, 48x48 or 64x64, and V/H Mixed Mode
- Support Full Size(16x16) and Half Size(8x16) Mode
- Font ROM Readable
- Support Align Function
- Support 4 Gray Layer Display
- Support Bold Font and Line Distance Setting
- Built-In 10-Bit ADC for Touch Panel
- Built-In 5-Bit DAC for Contrast Control
- Clock: 32KHz X'tal or External Clock
- Built-In a 5V to 3.3V DC-DC Converter
- Power Supply: 2.4~5V
- Package: Die, PQFP/LQPF 100Pins

3. Block Diagram

Figure 3-1 is the internal block diagram of RA8803. The RA8803 consists of Display RAM, 512Kbyte Font ROM, Command Registers, Analog to Digital Converter(ADC), Digital to Analog Converter(DAC), Display Timing Generator(DTG) and Microprocessor interface. Figure 3-2 is the internal block diagram of RA8822. The major difference of RA8803 and RA8822 is the Display RAM size. The RA8803 built-in two 9.6Kbyte display RAM, and RA8822 built-in two 4.8Kbyte RAM. Figure 3-3 is the system block for application of RA8803 and RA8822.

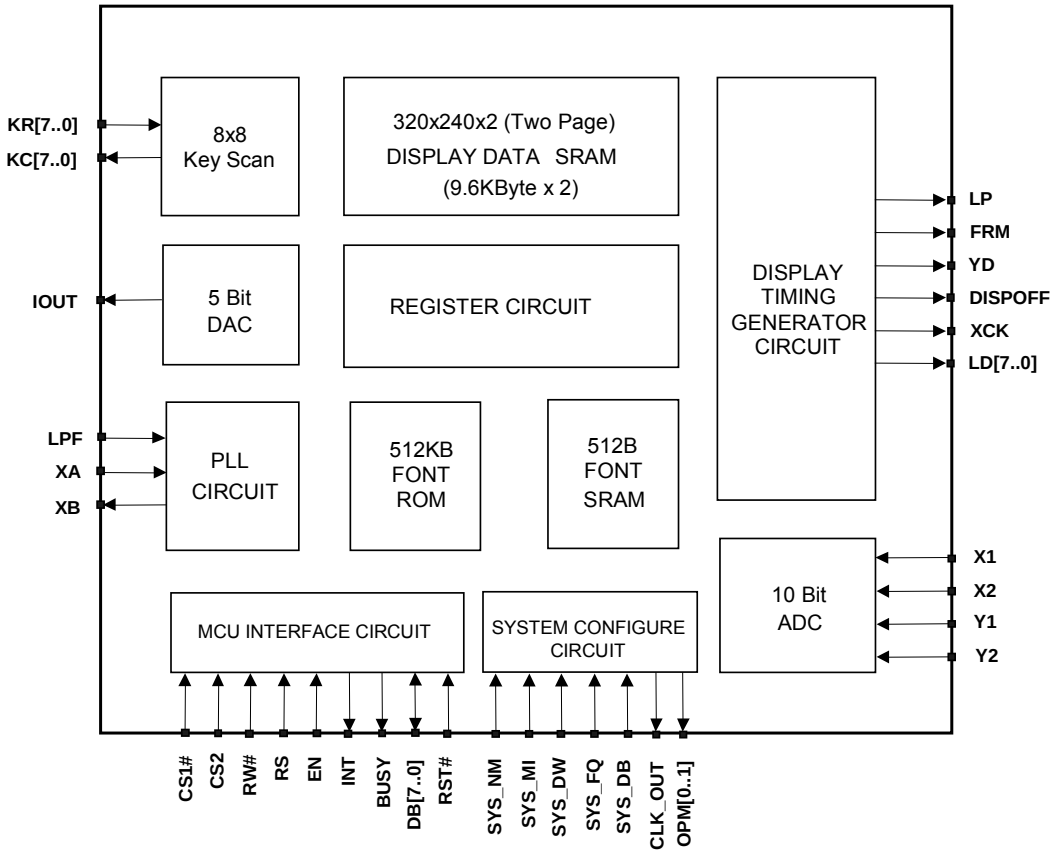

Figure 3-1: RA8803 Block Diagram

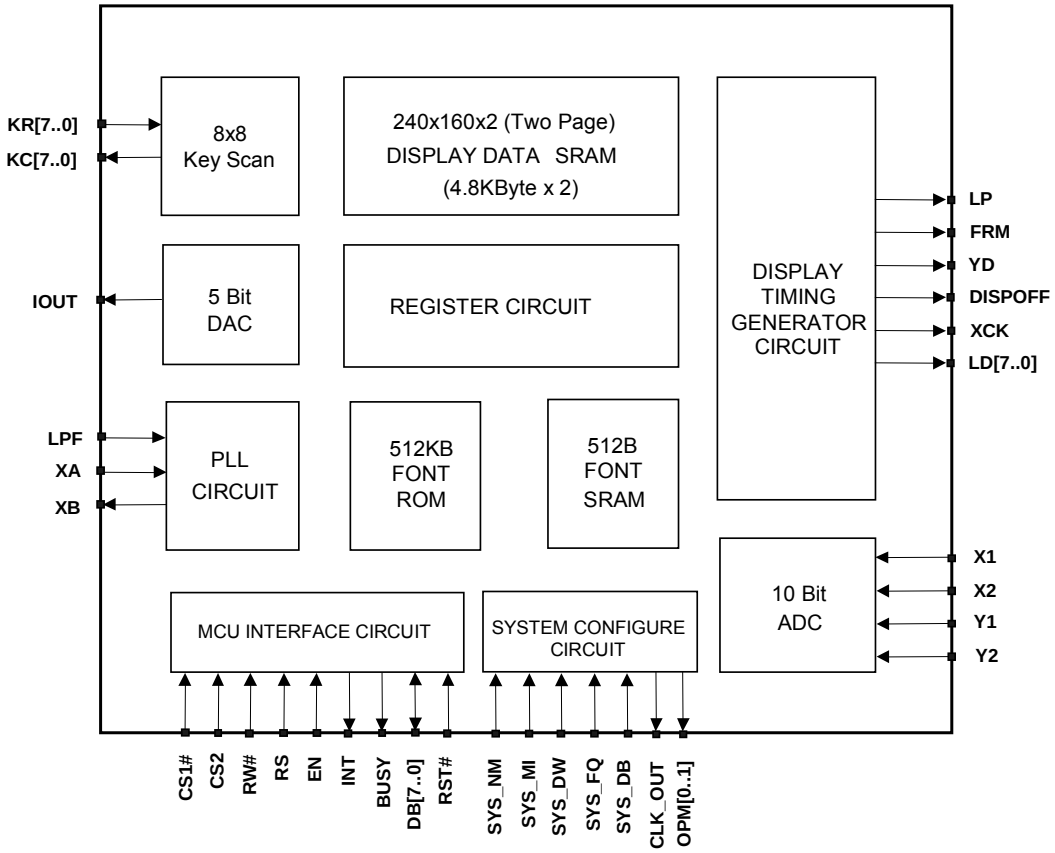

Figure 3-2: RA8822 Block Diagram

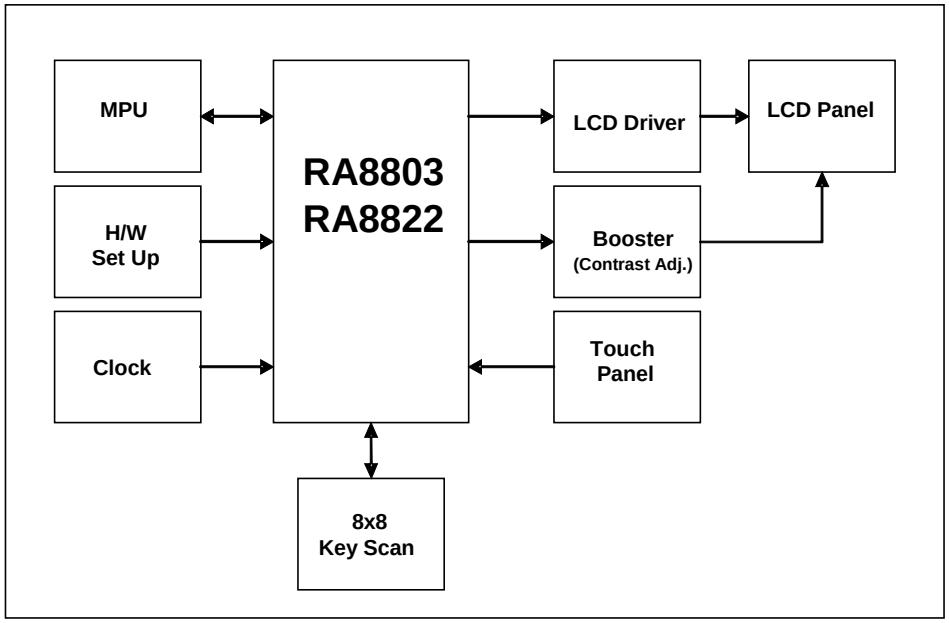

Figure 3-3: RA8803/8822 System Block Diagram

4. Pin Definition

4-1 MPU Interface

Pin Name	I/O	Description
DB[7..0]	I/O	**Data Bus** These are data bus for data transfer between MPU and RA8803/8822. The high nibble DB[7..4] should be floating when 4-bit data bus mode is used.
EN (RD#)	I	**Enable/Read Enable** When MPU I/F is 8080 series, this pin (RD#) is used as data read, active low. When MPU I/F is 6800 series, this pin (EN) is used as Enable, active high.
R/W# (WR#)	I	**Write/Read-Write** When MPU I/F is 8080 series, this pin (WR#) is used as data write, active low. When MPU I/F is 6800 series, this pin(R/W#) is used as data read/write control. Active high for read and active low for write.
RS	I	**Register/Memory Select** The MPU will access Register when RS is Low and access Data Memory when RS is High. Usually connect to MPU address bus A0.
CS1# CS2	I	**Chip Select** The RA8803/8822 is active when CS1# is low and CS2 is high
INT	O	**Interrupt Signal** This is an interrupt output to indicate the status of RA8803/88822. It could be setup active high or low.
BUSY	O	**Busy Signal** This is a busy output to indicate the RA8803/88822 is in busy state. It could be setup active high or low. If setup active high, the RA8803/8822 can't be access when BUSY pin is high. It's should be connected to MPU I/O input. The MPU have to poll this pin before accessing RA8803/8822.

4-2 LCD Driver Interface

Pin Name	I/O	Description
YD	O	**Start Signal of LCD Per Frame** YD is the frame start signal.
FRM	O	**Control Signal of LCD AC Wave** This signal controlt the Level Shift of LCD driver. Normally inputs a frame

		inversion signal.
LP	O	**LCD Common Latch** This is a latch signal for LCD driver to latch the Common data.
XCK	O	**LCD Clock** This is a shift clock signal for LCD driver.
DISPOFF	O	**LCD Display OFF** This signal is used to control the LCD Display ON or OFF.
LD[7..0]	O	**LCD Driver Data Bus** When 8-bit LCD driver IC is used. LD[7..0] are connected to LCD driver data bus. When 4-bit CPU is used, LD[3..0] are connected to LCD driver data bus and keep LD[7..4] floating.

4-3 Clock Interface

Pin Name	I/O	Description
LPF	I	**Low Pass Filter Input** This is a low pass filter input. Please refer the circuit of application note.
XA	I	**X'tal Input** In internal clock mode, this pin connects to external X'tal(32768Hz). In external clock mode, this is an input of external clock.
XB	O	**X'tal Output** This pin connects to external X'tal(32768Hz).

4-4 Peripheral Interface

Pin Name	I/O	Description
RST#	I	**Reset Signal** This is a reset signal used to reset RA8803/8822. Active low.
X1	I	**Touch Panel Input** This is connecting to the left pin(XL) of 4-wire touch panel.
X2	I	**Touch Panel Input** This is connecting to the right pin(XR) of 4-wire touch panel.
Y1	I	**Touch Panel Input** This is connecting to the top pin(YU) of 4-wire touch panel.
Y2	I	**Touch Panel Input** This is connecting to the bottom pin(YD) of 4-wire touch panel.
IOUT	O	**DAC Current Output** DAC current source output used to contrast voltage control. This pin is tri-state when DAC disbale.
KR[7..0]	I	**Key Pad Input**

		These pins are keypad inputs.
KC[7.0]	O	**Key Pad Output** These pins are keypad outputs.
CLK_OUT	O	**Clock Output** This is system clock output pin.
SYS_NM	I	**Test Pin** This is a test pin. Normally it connects to high.
SYS_FQ	I	**System Clock Select** This pin is used to select clock source. Pull Low (0) : X'tal/PLL Mode. Pull High(1) : External Clock. When SYS_FQ is Pull Low, then Internal oscillator and PLL are enable, only one external 32Khz X'tal need. When SYS_FQ is Pull High, then the system clock is from pin "XA".
SYS_DW	I	**LCD Driver Data Bus Select** This pin is used to select data bus of LCD driver is 8-Bit or 4-Bit: Pull Low(0) : 4-Bit Pull High(1) : 8-Bit When SYS_DW is Pull Low, then the LCD driver data bus Is 4-Bit. When SYS_DW is Pull High, then the LCD driver data bus is 8-Bit.
SYS_MI	I	**MPU Type Select** This pin is used to select MPU type: Pull Low(0) : I8080 Series Pull High(1) : M6800 Series When SYS_MI is Pull Low, then the MPU Interface of RA8803/8822 is suppported I8080. When SYS_MI is Pull High, then the MPU Interface of RA8803/8822 is supported M6800.
SYS_DB	I	**8080 MPU Data Bus Select** This pin is used to select data bus of 8080 MPU is 4-Bitor 8-Bit: Pull Low(0) : 4-Bit Pull High(1) : 8-Bit When SYS_DB is Pull Low, then the 8080 MPU Interface of RA8803/8822 is supported 4-Bit. When SYS_DB is Pull High, then the 8080 MPU Interface of RA8803/8822 is supported 8-Bit.

<table>
<tr>
<td>OPM0
OPM1</td>
<td>O</td>
<td>Operation Status of Current Command
These two pins are the feedback from RA8803/8822 while MPU release a Read or Write command to RA8803/8822. The MPU could know the status of RA8803/8822.
<table>
<tr><th>OPM0</th><th>OPM1</th><th>State</th></tr>
<tr><td>1</td><td>0</td><td>MPU is reading data from RA8803/8822.</td></tr>
<tr><td>1</td><td>1</td><td>MPU is writing data to RA8803/8822.</td></tr>
<tr><td>0</td><td>X</td><td>RA8803/8822 did not receive command or read a valid commend.</td></tr>
</table>
Normally the system does not need to use these two pins. And keep floating for not use.</td>
</tr>
</table>

4-5 Power

Pin Name	I/O	Description
VDD5	I	**5V Power** This is the input of 5V to 3.3V DC to DC Converter. If it connects to 5V power then the pin VDD3 will generate 3.3V power for internal cells and external device. If the system uses 3.3V power only, then keep this pin floatting.
VDD3	I/O	**3.3V Power** If the pin VDD5 connects to 5V power then this pin will generate 3.3V power for internal cells and external device. If the system uses 3.3V power only, then connect this pin to external 3.3V power directly.
VDDP	I	**I/O Power**
AVDD	I	**Analog Power of ADC for Touch Panel Controller**
GND GNDP	I	**Ground**
AGND	I	**Analog Ground of ADC for Touch Panel Controller**
TEST	I	**Test Pin** This pin is for test only and don't need to connect.

5. Register Description

5-1 Register List Table

Table 5-1 : Register Table

Reg. No	Reg. Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default Data
00h	WLCR	R/W	PW1	PW0	SR	--	CG	DP	DK	DV	C9h
01h	MISC	R/W	--	CKN	--	PLR	--	--	CKB1	CKB0	F0h
02h	APSR	R/W	--	--	SP1	SP0	OAR	--	SRFS	--	10h
03h	ADSR	R/W	--	--	--	--	DADR	AUCM	AUSG	SGCM	80h
10h	WCCR	R/W	ARI	ALG	WDI	WBC	AWI	CP	CK	CSD	6Fh
11h	DWLR	R/W	CR3	CR2	CR1	CR0	DY3	DY2	DY1	DY0	22h
12h	MAMR	R/W	GIM	RM2	RM1	RM0	OP1	OP2	WM1	WM0	91h
20h	AWRR	R/W	--	--	X5	X4	X3	X2	X1	X0	27h
21h	DWRR	R/W	--	--	A5	A4	A3	A2	A1	A0	27h
30h	AWBR	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	EFh
31h	DWBR	R/W	B7	B6	B5	B4	B3	B2	B1	B0	EFh
40h	AWLR	R/W	--	--	SS5	SS4	SS3	SS2	SS1	SS0	00h
41h	DWLR	R/W	--	--	C5	C4	C3	C2	C1	C0	00h
50h	AWTR	R/W	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
51h	DWTR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	00h
60h	CPXR	R/W	--	--	RS5	RS4	RS3	RS2	RS1	RS0	00h
61h	BGSG	R/W	--	--	DS5	DS4	DS3	DS2	DS1	DS0	00h
70h	CPYR	R/W	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00g
71h	BGCM	R/W	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	00h
72h	EDCM	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	EFh
80h	BTMR	R/W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	33h
81h	FRCA	R/W	--	--	--	--	--	--	--	--	00h
90h	SCCR	R/W	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0	04h
91h	FRCB	R/W	--	--	--	--	--	--	--	--	00h
A0h	INTR	R/W	INK	INT	INX	INY	MSK	MST	MSX	MSY	00h
A1h	KSCR	R/W	KEN	KSZ	KDT1	KDT0	--	KF2	KF1	KF0	00h
A2h	KSDR	RO	KS7	KS6	KS5	KS4	KS3	KS2	KS1	KS0	00h
A3h	KSER	RO	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	00h
B0h	INTX	R/W	--	--	IX5	IX4	IX3	IX2	IX1	IX0	27h
B1h	INTY	R/W	IY7	IY6	IY5	IY4	IY3	IY2	IY1	IY0	EFh
C0h	TPCR	R/W	AZEN	AZOE	--	SCAN	AS3	AS2	AS1	AS0	00h
C1h	TPSR	R/W	ARDY	ADET	1	1	AF1	AF0	--	--	0Fh
C8h	TPXR	RO	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C9h	TPYR	RO	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
CAh	TPZR	RO	TPX1	TPX0	--	--	TPY1	TPY0	--	--	00h
D0h	LCCR	R/W	DZEN	--	--	DAC4	DAC3	DAC2	DAC1	DAC0	8Fh
E0h	PNTR	R/W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	00h
F0h	FNCR	R/W	TNS	BNK	RM1	RM0	FDA	ASC	ABS1	ABS0	92h
F1h	FVHT	R/W	FH1	FH0	FV1	FV0	1	1	1	1	0Fh

5-2 Register Description

REG [00h] Whole Chip LCD Controller Register (**WLCR**)

Bit	Description	Text/Graph	Default	Access
7-6	**Power Mode** 1 1 : Normal Mode. All of the functions of RA8803/8822 are available in this mode. 0 0 : Off Mode. When RA8803/8822 is in off mode, all of functions enter power-off mode, except the wake-up trigger block. If wake-up event occurred, RA8803/8822 would wake-up and return to Normal mode.	--	3h	R/W
5	**Software Reset:** 1 : Reset all registers except flushing RAM 0 : Normal Operation	--	0h	R/W
4	Reserved.	--	0h	R/W
3	**Display Mode Selection** 1 : Character Mode. The written data will be treated as a GB/BIG/ASCII code. 0 : Graphical Mode. The written data will be treated as a bit-map pattern.	--	1h	R/W
2	**Set Display On/Off Selection** The bit is used to control LCD Driver Interface signals -- DISP_OFF. 1 : DISP_OFF pin output high(Display On). 0 : DISP_OFF pin output low(Display Off).	Text/Graph	0h	R/W
1	**Blink Mode Selection** 1 : Blink Full Screen. The blink time is set by register BTMR. 0 : Normal Display.	Text/Graph	0h	R/W
0	**Inverse Mode Selection** 1 : Normal Display 0 : Inverse Full Screen. It will cause the display inversed.	Text/Graph	1h	R/W

REG [01h] Misc. Register (**MISC**)

Bit	Description	Default	Access
7	Reserved.	1h	R/W
6	**Clock Output (Pin CLK_OUT) Control** 1 : Enable 0 : Disable	1h	R/W
5	Reserved.	1h	R/W
4	**Interrupt (INT) and Busy Polarity** 1 : Set Active High	1h	R/W

	0 : Set Active Low		
3-2	Reserved.	0h	R/W
1-0	**Clock Speed Selection** 0 0 : 3MHz 0 1 : 4MHz 1 0 : 8MHz 1 1 : 12MHz	0h	R/W

REG [02h] Advance Power Setup Register (**APSR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-4	**ROM/RAM Reading Speed** 0 0 : Speed0 (30ns@Vdd=3.3V) 0 1 : Speed1 (60ns@Vdd=3.3V) 1 0 : Speed2 (90ns@Vdd=3.3V) 1 1 : Speed3 (120ns@Vdd=3.3V)	1h	R/W
3	**Font ROM Readable for MPU** 1 : Enable 0 : Disable	0h	R/W
2	Reserved	0h	R/W
1	Scrolling Reset for Start 0 : Disable 1 : Enable	0h	R/W
0	Reserved	0h	R/W

REG [03h] Advance Display Setup Register (**ADSR**)

Bit	Description	Default	Access
7-4	Reserved	8h	R/W
3	**Set Display RAM Order (Byte)** 1 : Inverse Data of Byte 0 : Normal Mode	0h	R/W
2	**Common Auto Scrolling** 1 : Enable 0 : Disable	0h	R/W
1	**Segment Auto Scrolling** 1 : Enable 0 : Disable	0h	R/W
0	**Common or Segment Scrolling Selection** 1 : Segment Scrolling 0 : Common Scrolling	0h	R/W

	In Extension Mode(REG[12h] 的 bit[6:4] = “110” 或”111”), this bit must be high.		

REG [10h] Whole Chip Cursor Control Register (**WCCR**)

Bit	Description	Text/Graph	Default	Access
7	**Auto Increase Cursor Position in Reading DDRAM Operation.** 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	0h	R/W
6	**Chinese/English Character Alignment** 1 : Enable 0 : Disable The bit only valid in character mode, that can align full-size and half-size mixed font.	Text	1h	R/W
5	**Store Current Data to DDRAM** 1 : Store Current Data to DDRAM Directly 0 : Store Current Data to DDRAM Inversely	Text/Graph	1h	R/W
4	**Bold Font** (Character Mode Only) 1 : Bold Font 0 : Normal Font	Text	0h	R/W
3	**Auto Increase Cursor Position in Writing DDRAM Operation.** 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	1h	R/W
2	**Cursor Display** 1 : Set Cursor Display On 0 : Set Cursor Display Off	Text/Graph	1h	R/W
1	**Cursor Blinking** 1 : Blink Cursor. The blink time is determined by BTMR. 0 : Normal	Text/Graph	1h	R/W
0	**Cursor Width** 1 : Cursor width is auto adjust by input data. When half size font, the width is one bit(8 Pixel). When full size font, the width is two bit(16 Pixel). 0 : Cursor is fixed at one byte width(8 Pixel).	Text	1h	R/W

REG [11h] Distance of Words or Lines Register (**DWLR**)

Bit	Description	Default	Access
7-4	**Set Cursor Height**	2h	R/W
3-0	**Set Line Distance**	2h	R/W

REG [12h] Memory Access Mode Register (**MAMR**)

Bit	Description	Default	Access
7	**In Graphic Mode, Cursor Auto Shifting Direction** 1 : Horizontal moving first then Vertical. 0 : Vertical moving first then Horizontal.	1h	R/W
6-4	**Display Layer Selection** 0 0 1 : Only Show Page1 0 1 0 : Only Show Page2 0 1 1 : Show Two Layer Mode. The display rule depends on Bit3 and Bit2 as following. 0 0 0 : Gray Mode. In this mode, each pixel gray of LCD depends on the value of Page1 & Page2. Page1 Page2 Gray --- 0 0 Level1 1 0 Level2 0 1 Level3 1 1 Level4 1 1 0：Extension Mode(1), the panel will show both Page1 and Page2. The RA8803 is available for 640x240 dots panel, and RA8822 for 480x160 dots panel. 1 1 1：Extension Mode(2), the panel will show both Page1 and Page2. The RA8803 is available for 320x480 dots panel, and RA8822 for 240x320 dots panel.	1h	R/W
3-2	**Two Layer Mode Selection** 0 0 : Page1 RAM “OR” Page2 RAM 0 1 : Page1 RAM “XOR” Page2 RAM 1 0 : Page1 RAM “NOR” Page2 RAM 1 1 : Page1 RAM “AND” Page2 RAM Please refer to Figure 7-10 for more explanation.	0h	R/W
1-0	**MPU Read/Write Layer Selection** 0 0 : Access Page0 (512B SRAM) Display Data RAM. 0 1 : Access Page1 (9.6KB SRAM) Display Data RAM. 1 0 : Access Page2 (9.6KB SRAM) Display Data RAM. 1 1 : Access Page1 and Page2 Display Data RAM at the same time. The Page0 are used for create some temporary characters. Please refer to AP Note for more details.	1h	R/W

REG [20h] Active Window Right Register (**AWRR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Active Window Right Position** → Segment-Right	27h	R/W

Note: REG [20h, 30h, 40h, 50h] are used for the function of change the line and page. Users can use these four Registers to set a block as an active window. When data goes beyond the right boundary of active window (The value is set by REG [20h, 30h, 40h, 50h]), then the cursor will automatically change the line and write in data continuously. It means the cursor will move to the left boundary of active window, which is set by REG [40h]. When the data comes to the bottom line of the right side (set by REG [20h and 30h]), then the cursor will be moved to the first line of the left side automatically and continue to put in data. (set by REG [40h, 50h]).

REG [30h] Active Window Bottom Register (**AWBR**)

Bit	Description	Default	Access
7-0	**Active Window Bottom Position** → Common-Bottom	EFh	R/W

REG [40h] Active Window Left Register (**AWLR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Active Window Left Position** → Segment-Left	0h	R/W

REG [50h] Active Window Top Register (**AWTR**)

Bit	Description	Default	Access
7-0	**Active Window Top Position** → Common-Top	0h	R/W

REG [21h] Display Window Right Register (**DWRR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-0	**Set Display Window Right Position** → Segment-Right **Segment-Right = (Segment Number / 8) – 1** RA8803: If LCD panel resolution is 320*240, the value of the register is: (320 / 8) - 1 = 39 = 27h RA8822: If LCD panel resolution is 240*160, the value of the register is: (240 / 8) - 1 = 29 = 1Dh	27h	R/W

Note: REG[21h, 31h, 41h, 51h] are used to set Display Window Resolution. Users can set the viewing scope of Display RAM. Column Address of RA8803 can be set between 0~27h, and Row Address can be set between 0~EFh. Column Address of RA8822 can be set between 0~1Dh, and Row Address can be set between 0~9Fh. Users can set start and end address first, and then by adding shift function to present the

effect of rolling.

REG [31] Display Window Bottom Register (**DWBR**)

Bit	Description	Default	Access
7-0	**Display Window Bottom Position** → Common-Bottom **Common_ Bottom = LCD Common Number –1** RA8803: If LCD panel resolution is 320*240, the value of the register is: 240 – 1 = 239 = EFh RA8822: If LCD panel resolution is 240*160, the value of the register is: 160 – 1 = 159 = 9Fh	EFh	R/W

Note: Only when Common is 128, the Common_Bottom = LCD Common Number. Refer to the section 5-3.

REG [41] Display Window Left Register (**DWLR**)

Bit	Description	Default	Access
7-0	**Display Window Left Position** → Segment-Left Usually set “0h”.	0h	R/W

REG [51] Display Window Top Register (**DWTR**)

Bit	Description	Default	Access
7-0	**Display Window Top Position** → Common-Top Usually set “0h”.	0h	R/W

Note: For some registers setting, please refer the following rule:

1. DWRR≥ AWRR≥ CPXR≥ AWLR≥ DWLR
2. DWBR≥ AWBR≥ CPYR≥ AWTR≥ DWTR

REG [60h] Cursor Position X Register (**CPXR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Cursor Position of Segment**	0h	R/W

REG [61h] Begin Segment Position Register (**BGSG**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-0	**Segment Start Position of Scrolling Mode**	0h	R/W

REG [70h] Cursor Position Y Register (**CPYR**)

Bit	Description	Default	Access
7-0	**Cursor Position of Common**	0h	R/W

REG [71h] Scrolling Action Range, Begin Common Register (**BGCM**)

Bit	Description	Default	Access
7-0	**Common Start Position of Scrolling Mode**	0h	R/W

REG [72h] Scrolling Action Range END Common Register (**EDCM**)

Bit	Description	Default	Access
7-0	**Common Ending Position of Scrolling Mode**	EFh	R/W

REG [80h] Blink Time Register (**BTMR**)

Bit	Description	Default	Access
7-0	**Cursor Blink Time** Blinking Time = Bit [7..0] x (1/Frame_Rate) The setup of Frame Rate is depends on the LCD panel.	33h	R/W

REG [81h] Frame Rate Polarity Change at Common_A Register (**FRCA**)

Bit	Description	Default	Access
7-0	**Reserved** If the Common number of module is 128 then suggest set to “0Ch”. Refer the Section 5-3.	0h	R/W

REG [91h] Frame Rate Polarity Change at Common_B Register (**FRCB**)

Bit	Description	Default	Access
7-0	**Reserved**	0h	R/W

REG [90h] Shift Clock Control Register (**SCCR**)

Bit	Description	Default	Access
7-0	**Shift Clock Cycle** **SCCR = (SCLK x DW) / (Seg x Com x FRM)** SCLK : RA8803/8822 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel(Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel) FRM : Frame Rate of LCD Panel(Unit : Hz)	4h	R/W

	Note: SYS_DW=0, If LCD Data Bus is 4it then SCCR has to ≥ 4. SYS_DW=1, If LCD Data Bus is 8it then SCCR has to ≥ 2.		

REG [A0h] Interrupt Setup & Status Register (**INTR**)

Bit	Description	Default	Access
7	**Key Scan Interrupt Flag** 1 : Key Scan Detects Key Input 0 : Key Scan doesn't Detect Key Input	0h	R (Read Clear)
6	**Touch Panel Detect** 1 : Touch Panel Touched 0 : Touch Panel Untouched	0h	R (Read Clear)
5	**Cursor Column Status** 1 : The Cursor Column is equal to INTX 0 : The Cursor Column is not equal to INTX	0h	R (Read Clear)
4	**Cursor Row Status** 1 : The Cursor Row is equal to INTY 0 : The Cursor Row is not equal to INTY	0h	R (Read Clear)
3	**Key Scan Interrupt Mask** 1 : Enable Key Scan Interrupt. Enable BUSY signal. 0 : Disable Key Scan Interrupt	0h	R/W
2	**Touch Panel Interrupt Mask** 1 : Generate interrupt output if touch panel was detected. Enable BUSY signal. 0 : Don't generate interrupt output if touch panel was detected.	0h	R/W
1	**Register[B0h] INTX Event Mask** 1 : Enable INTX Interrupt. Enable BUSY signal. 0 : Disable INTX Interrupt	0h	R/W
0	**Register[B1h] INTY Event Mask** 1 : Enable INTY Interrupt. Enable BUSY signal. 0 : Disable INTY Interrupt	0h	R/W

Note: Any Bit of Bit3~Bit0 set to "1", then the BUSY Signal will be enable. The Polarity of BUSY depends on the Bit4 of Register [01h].

REG [A1h] Key Scan Controller Register (**KSCR**)

Bit	Description	Default	Access
7	**Key Scan Enable Bit** 1 : Enable 0 : Disable	0h	R/W
6	**Key Scan Matrix Selection** 1 : 4x4 Matrix	0h	R/W

	0 : 8x8 Matrix		
5-4	**Key Scan Data Sampling Times** 0 0 : 2h 0 1 : 4h 1 0 : 8h 1 1 : 16h	0h	R/W
3	Reserved	0h	R/W
2-0	**Key Scan Frequency Selection** 0 0 0 : 2 x FRM 0 0 1 : 4 x FRM 0 1 0 : 8 x FRM 0 1 1 : 16 x FRM 1 0 0 : 32 x FRM 1 0 1 : 64 x FRM 1 1 0 : 128 x FRM 1 1 1 : 256 x FRM	0h	R/W

REG [A2h] Key Scan Data Register (**KSDR**)

Bit	Description	Default	Access
7-0	**Key Scan KC[7~0] Output**	0h	R

REG [A3h] Key Scan Data Expand Register (**KSER**)

Bit	Description	Default	Access
7-0	**Key Scan KR[7~0] Input**	0h	R

REG [B0h] Interrupt Column Setup Register (**INTX**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Column Address of Interrupt** If Cursor Position X Register (CPXR)=INTX, then an interrupt occurred.	27h	R/W

REG [B1h] Interrupt Row Setup Register (**INTY**)

Bit	Description	Default	Access
7-0	**Row Address of Interrupt** If Cursor Position Y Register (CPYR)=INTY, then an interrupt has occurred.	EFh	R/W

REG [C0h] Touch Panel Control Register (**TPCR**)

Bit	Description	Default	Access

7	**Touch Panel Enable Bit** 1 : Enable 0 : Disable	1h	R/W
6	**Touch Panel Data Output Control** 1 : Enable the Touch Panel Data Output 0 : Disable the Touch Panel Data Output	1h	R/W
5	**Reserved**	0h	R/W
4	**Touch Panel Scan** 1 : Disable 0 : Enable	1h	R/W
3-0	**Switch Control of Touch Panel** Bit3: control SW3 ON/OFF(1/0) Bit2: control SW2 ON/OFF(1/0) Bit1: control SW1 ON/OFF(1/0) Bit0: control SW0 ON/OFF(1/0)	Fig. 6-6	R/W

REG [C1h] Touch Panel Status Register (**TPSR**)

Bit	Description	Default	Access
7	**ADC Data Convert State** 1 : Convert Complete 0 : Convert Incomplete	0h	R
6	**Touch Event Indicate** 1 : Touched 0 : Un-touch	0h	R
5	This bit Must be “1” when system initial.	0h	R/W
4	This bit Must be “1” when system initial.	0h	R/W
3-2	**ADC Convert Speed** 0 0 : SCLK/32 0 1 : SCLK/64 1 0 : SCLK/128 1 1 : SCLK/256	2h	R/W
1-0	**Reserved**	2h	R/W

REG [C8h] Touch Panel Segment High Byte Data Register (**TPXR**)

Bit	Description	Default	Access
7-0	**Touch Panel Segment Data Bit[9..2]**	80h	R

REG [C9h] Touch Panel Common High Byte Data Register (**TPYR**)

Bit	Description	Default	Access
7-0	**Touch Panel Common Data Bit[9..2]**	80h	R

REG [CAh] Touch Panel Segment/Common Low Byte Data Register (**TPZR**)

Bit	Description	Default	Access
7-6	**Touch Panel Segment Data Bit[1..0]**	0h	R
5-4	Reserved	0h	--
3-2	**Touch Panel Common Data Bit[1..0]**	0h	R
1-0	Reserved	0h	--

REG [D0h] LCD Contrast Control Register (**LCCR**)

Bit	Description	Default	Access
7	**DAC Function** 1 : Disable 0 : Enable	1h	R/W
6-5	Reserved	0h	--
4-0	**DAC Driving Current** 0 0 0 0 0b → 0μA±0.2μA (Min. Current) : : 1 1 1 1 1b → 540μA±140 μA (Max. Current)	0Fh	R/W

REG [E0h] Pattern Data Register (**PNTR**)

Bit	Description	Default	Access
7-0	**(1) Data Written to DDRAM** When REG[F0h] bit3 is '1', it will read the data from Register [E0h] and fill the whole DDRAM. After the movement of filling the Active window, REG [F0h] bit3 will become "0". **(2) Display Times of Gray Mode** For Gray Mode(Register MAMR bit[6..4] = 000), These register used to control the display times. If the frame rate is fixed, the number of "1" and "0" are represent the display ratio of 1 and 0. Please see Chapter 7-10 and AP Note 9-23 for more description.	0h	R/W

REG [F0h] Font Control Register (**FNCR**)

Bit	Description	Text/Graph	Default	Access
7	**Font ROM Transfer Circuit** 1 : Enable 0 : Bypass	--	1h	R/W
6	When bit5~4 set as "00" → ROM Mode0, this bit could be used to select the upper or lower part of 256KB ROM. 1 : Select lower part of 256KB ROM	--	0h	R/W

	0 : Select upper part of 256KB ROM			
5-4	**Select Font ROM Type** 0 0 : Select GB font ROM (256KB, Mode0) 0 1 : Select BIG5 font ROM (512KB, Mode1) 1 0 : Support GB font ROM (512KB, Mode2)	--	1h	R/W
3	**Fill PNTR Data to DDRAM** 1 : Fill Data to DDRAM Enable 0 : No Action When this bit is "1", RA8803/8822 will automatically read PNTR data, and fill it to DDRAM (Range:[AWLR, AWTR] ~ [AWRR, AWBR]), and then this bit will be cleaned to "0".	Graph	0h	R/W
2	**ASCII Code Selection** 1 : All input data will be decoded as ASCII (00~FFh) 0 : The RA8803/8822 will check the first byte data first. If the first byte is 00~9Fh then regarded as ASCII (Half-size). If first byte is A0~FFh then regarded as GB/BIG5 (Full-size).	Text	0h	R/W (Auto Clear)
1-0	**ASCII Blocks Select** 0 0 : Map to ASCII block 0, Latin_1 0 1 : Map to ASCII block 1, Latin_2 1 0 : Map to ASCII block 2, Latin_3 1 1 : Map to ASCII block 3, Latin_4	--	2h	R/W

REG [F1h] Font Size Control Register (**FVHT**)

Bit	Description	Default	Access
7-6	**Set Character Horizon Size** 0 0 : One Time 0 1 : Two Times 1 0 : Three Times 1 1 : Four Times	0h	R/W
5-4	**Set Character Vertical Size** 0 0 : One Time 0 1 : Two Times 1 0 : Three Times 1 1 : Four Times	0h	R/W
3-0	**Reserved**	Fh	R/W

5-3 Registers for Display Resolution

Normally the REG[40h], REG[50h], REG[41h] and REG[51h] set to "00h". And the content of REG[20h], REG[30h], REG[21h] and REG[31h] are depend on the resolution of LCD module. The following are reference table of different LCD module.

Table 5-2：Registers Setting for LCM Resolution

Segment	Common	REG[20h] AWRR	REG[30h] AWBR	REG[21h] DWRR	REG[31h] DWBR
160	**80**	13h	4Fh	13h	4Fh
160	**128**	13h	7Fh	13h	**80h**
160	**160**	13h	9Fh	13h	9Fh
240	**64**	1Dh	3Fh	1Dh	3Fh
240	**128**	1Dh	7Fh	1Dh	**80h**
240	**160**	1Dh	9Fh	1Dh	9Fh
320	**240**	27h	EFh	27h	EFh

Note: Normally the REG[31h] value is Common-1, only when Common is 128, then the REG[31h] is 80h. If Common is 128 and keep the REG[31h] to 7Fh, then you have to set up the REG[81h] to 0Ch.

6. Function Description

6-1 MPU Interface

The RA8803/8822 support 8080 or 6800 compatible MPU interface. When the pin SYS_MI is pull low then the MPU interface is set to 8080 compatible. If SYS_MI pull high then the MPU interface is defined as 6800 compatible.

And the pin SYS_DB is used to select the 8080 MPU data bus is 4-Bit or 8-Bit. When SYS_DB pull low, then the data bus for data transition is 4-Bit. If pin SYS_DB pull high, the data transition is 8-Bit. The option of 4-Bit or 8-Bit data bus is for 8080 MPU only. Of course, if used 4-Bit interface then the 8080 MPU has to take double time to communicate with RA8803/8822.

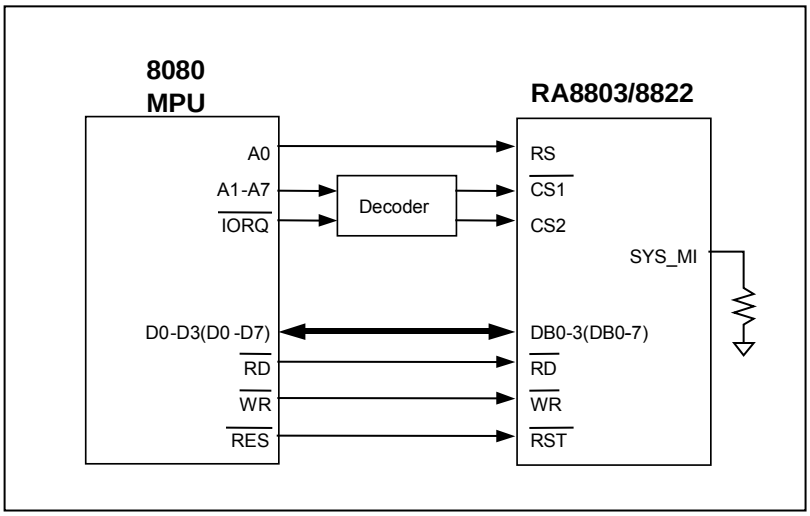

Figure 6-1: 8080 (4/8-Bit) MPU Interface

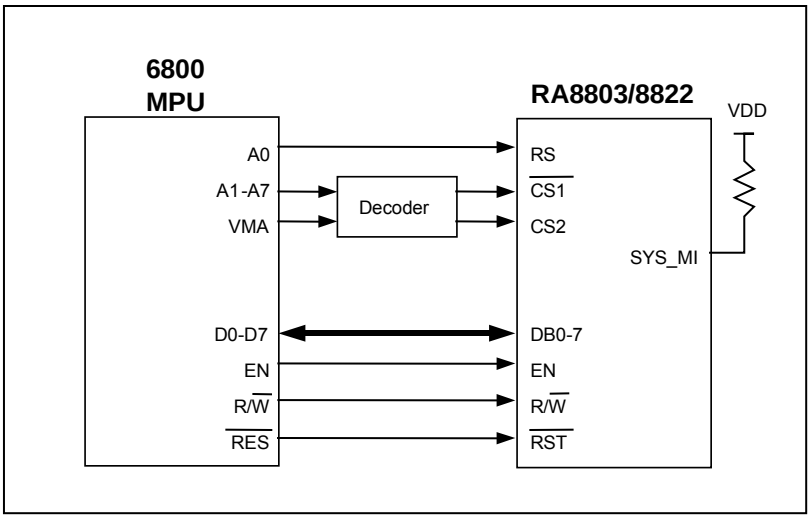

Figure 6-2: 6800 (8-Bit Only) MPU Interface

6-2 Command / Decoder Registers

This circuit store and implement the command from MPU Interface. The register WLCR, MISC, APSR and ADSR are used for system setting. Registers WCCR, DWLR, CPXR and CPYR are used for cursor feature. Registers AWRR, AWBR, AWLR and AWTR are used for setting the range of active window. The RA8803 set up registers – DWRR, DWBR, DWLR and DWTR to support (0,0) ~ (320,240) pixel LCD Panel. And RA8822 use these registers to support (0,0) ~ (240,160) pixel LCD Panel.

Registers INTR, INTX and INTY provide the interrupt related functions to reduce MPU's loading. The registers KSCR, KSDR and KSER are used for Key Scan features. The others hardware such as ADC(controlled by Registers TPSR, TPXR, TPYR, TPZR) and DAC(controlled by Register LCCR) are also controlled by these circuit and related registers.

6-3 Display Data RAM (DDRAM)

The RA8803 embedded two 9.6Kbyte display RAM for two layers display. It supports the maximum resolution of LCD panel is 320Column x 240Row. RA8822 embedded two 4.8Kbyte display RAM and support 240Column x 160Row for maximum resolution. The RA8803/8822 support both text and graphics mode. The user could switch both two modes at any time.

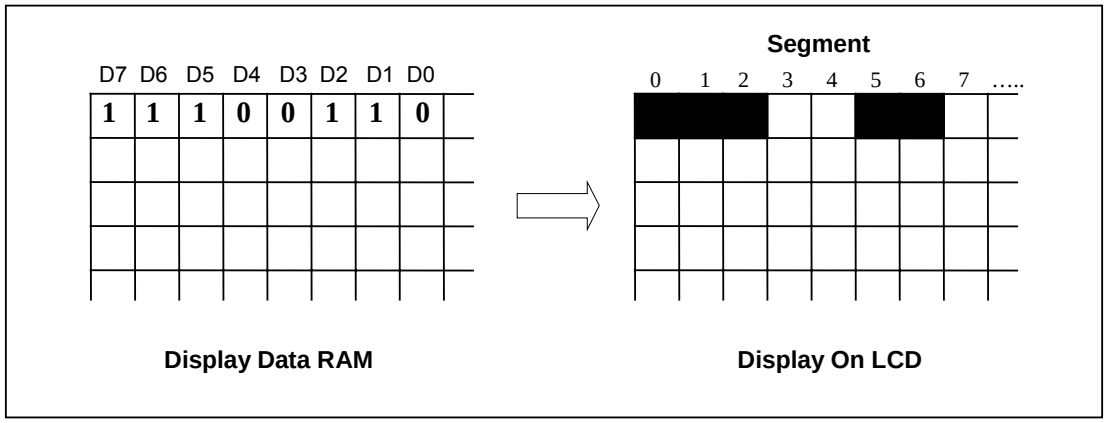

Figure 6-3: Display Data to LCD Map

6-4 Display Timing Generator(DTGC)

The main function of DTGC is to generate Frame (FRM), Latch Pulse (LP), YD and Data Bus signals for external LCD driver IC. RA8803/8822 could both support 4-bit and 8-bit LCD driver interface. SYS_DW is for LCD driver data bus selection. If SYS_DW pull high then 8-bit LCD driver is used. If pull low then 4-bit LCD driver is used.

6-5 LCD Display

RA8803 support many different resolution of LCD panel. The maximum resolution - 320x240 dots that means 20x 15 full size Chinese character(RA8803/8822 define a Chinese character is 16x16 dots and ASCII is 8x16). Due to the smaller display RAM size, the maximum resolution of RA8822 is 240x160

dots -- 15x 10 Chinese character. For different resolution of panel, RA8803/8822 could change the setting of some registers like DWRR, DWBR, DWLR and DWTR to modify display window size. And use registers AWRR, AWBR, AWLR and AWTR to change the active window size.

For example, if use RA8803 to support 320x240 LCD panel, then the related register setting are as following:

DWRR = (320 / 8) - 1 = 39 = 27h
DWBR = 240 – 1 = 239 = EFh
DWLR = 0
DWTR = 0

The active window range is less than display window. So user has to care the rule as following:

1. DWRR≥ AWRR≥ CPXR≥ AWLR≥ DWLR
2. DWBR≥ AWBR≥ CPYR≥ AWTR≥ DWTR

6-6 Font ROM and Font Size

RA8803/8822 embedded 512KByte Font ROM, having the standard and special fonts(16x16) of BIG5, GB, and ASCII(8x16) code. It can support the display 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display.

RA8803/8822-T: Built-in 13,094 standard Traditional Chinese character, 408 special character and 4 blocks ASCII character.

RA8803/8822-S: Built-in 7,602 standard Simple Chinese character, 408 special character and 4 blocks ASCII character.

Besides that, it also features with bigger Font size. Users can use Register FVHT to set the Font size to 16x32, 16x48, 16x64, 32x16, 32x32, 32x48, 32x64, 48x16, 48x32, 48x48, 48x64, 64x16, 64x32, 64x48 and 64x64 for maximum.

The RA8803/8822 also provide Font ROM readable feature. The MPU could read the bitmap of each font from Font ROM for other application.

6-7 System Clock

RA8802/8803 could depend on SYS_FQ Pull High or Low to decide the clock source. Pull Low is using internal PLL and external 32KHz crystal, and Pull High is using external CLK input as clock source.

6-7-1 PLL/OSC Circuit

RA8803/8822 is built in PLL/OSC circuits. By using an external 32KHz crystal, internal PLL could generate higher clock which system needs. When choosing a different resolution of panel, users could set Register CKB1 and CKB0 for system clock selection to reduce the power consumption.

Figure 6-4 is the PLL & OSC application circuit.

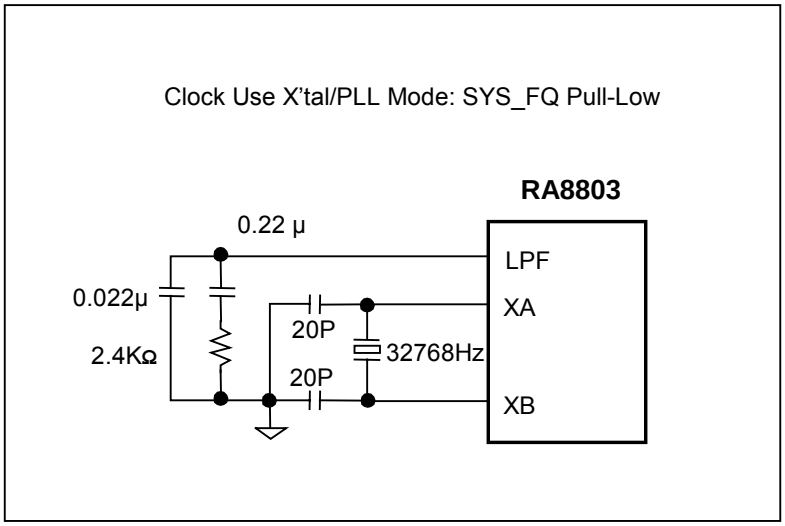

Figure 6-4: PLL Application Circuit

6-7-2 External Clock

RA8803/8822 can accept external CLK for system clock source. Directly connecting to XA, and keep XB, LPF floating.

6-8 DAC

The RA8803/8822 built-in one 5-bit fixed current type Digital-to-Analog Converter (D/A). This DAC will generate different current output through the setting of register. So users can use it to control the external booster and adjust the LCD voltage to control the brightness of LCD panel. The DAC out put "IOUT" is tri-state when DAC disable.

6-9 ADC

The RA8803/8822 built in a 10-Bit ADC and some control circuits to easily interface to 4-wries analog resistive touch screens. The users only need to connect the touch panel signals -- XL, XR, YU, and YD to RA8803/8822. The RA8803/8822 will continuous to monitor the screen and waiting for a touch. When the screen was being touched, the RA8803/8822 will performs analog to digital conversion to determine the location of the touch, stores the X and Y locations in the registers, and can issues an interrupt for MPU.

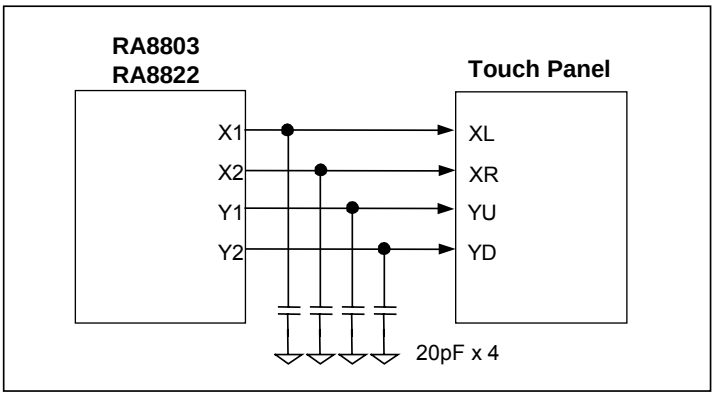

Figure 6-5: RA8803/8822 Touch Panel Circuit

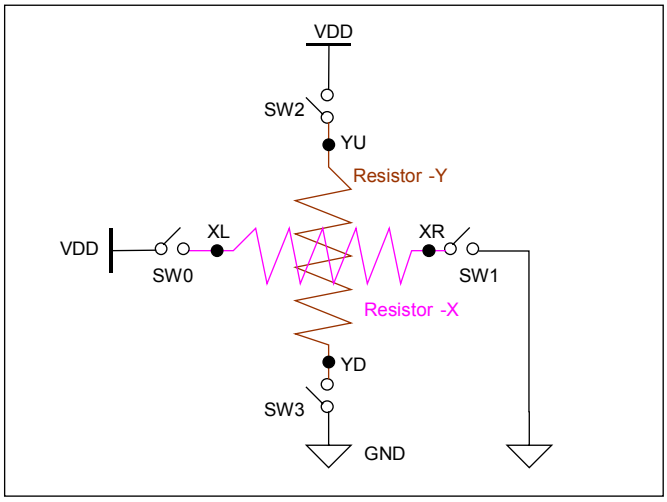

Figure 6-6: Control Switch of Touch Panel

6-10 Key Scan

RA8803/8822 features with Key Scan circuit, and could be used as Keyboard function. It will help to integrated the system circuit that includes keyboard application. The related Registers are KSCR, KSDR, and KSER.

6-11 Interrupt and Busy

RA8803/8822 provides an Interrupt signal (INT) to indicate four possible interrupts:

- If Cursor Position X Register (CPXR) = INTX, a interrupt has occurred
- If Cursor Position Y Register (CPYR) = INTY, a interrupt has occurred
- Interrupt occurs when Touch Panel is touched
- Key scan enable and key pressed

These four interrupts can be enabled or disabled respectively. The register [A0h] INTR controls the setup of interrupt mask and record the status.

The RA8803/8822 also provides a Busy signal. When BUSY Flag is “1”, which means RA8803/8822 is in busy status that RA8803/8822 couldn’t access data of DDRAM but still accept the commands from registers. If BUSY is ‘0’, which means RA8803/8822 is in idle state.

Normally, this BUSY pin is connected to MPU I/O input, and then MPU have to monitor this pin before accessing RA8803/8822.

6-12 Power

6-12-1 Power Architecture

The power architecture of RA8803/8822 is show as Figure 6-7. The I/O power is VDDP and GNDP. The analog power for internal ADC are AVDD and AGND. The RA8803/8822 built-in a 5V to 3V DC/DC Converter. The input power of this Converter is VDD5, and VDD3 is the output. VDD3 supply the power of internal core and DAC. If the system uses 3V only, then connect the 3V power to VDDP, VDD3 and AVDD directly. Please refer t to AP note Appendix B-2.

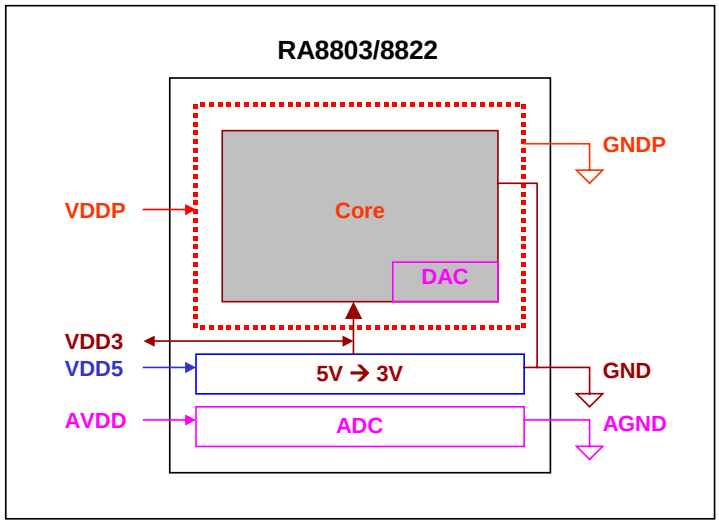

Figure 6-7: Power Architecture

6-12-2 Power Saving Mode

The RA8803/8822 provide two operation modes: Normal Mode and Off Mode. Please refer to Chapter 5-2 for Register WLCR explanation. When RA8803/8822 is under Off Mode, it can accept the following three methods to Wake-up.

1. Directly Command REG[00h], then it will return to Normal Mode
2. Touch event is detected
3. Key Scan is detected

6-13 ASCII Block Font Selection

RA8803/8822 built in four ASCII Font Blocks, and could be set by register ABS1 and ABS0. If users need special symbols or graphic, it could also be achieved by adjusting ROM Code. Please refer Application Note Chapter 9-21 for more detail.

6-14 Create Font

The RA8803/8822 embedded a 512Byte SRAM for user to create new character. The user could create 16 full size(16x16) Chinese font or special symbol in this memory. Please refer to AP Note for more details.

7. Display Functions

7-1 Text Mode

The text mode of RA8803/8822 supports full size(Chinese) and half size display. The full size character consists of 16x16 dots matrix and half size is 8x16 dots. The Figure 7-1 is an example to show the Full size and half size character.

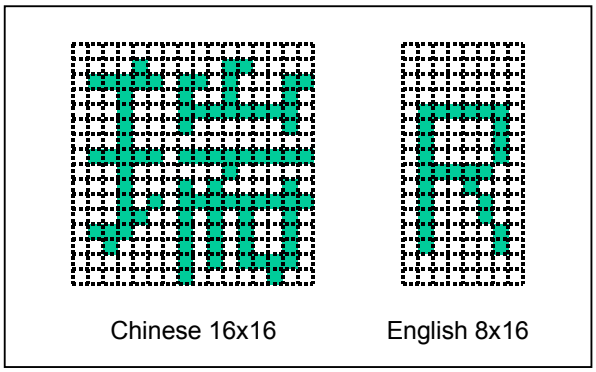

Figure 7-1: Full and Half Size Font

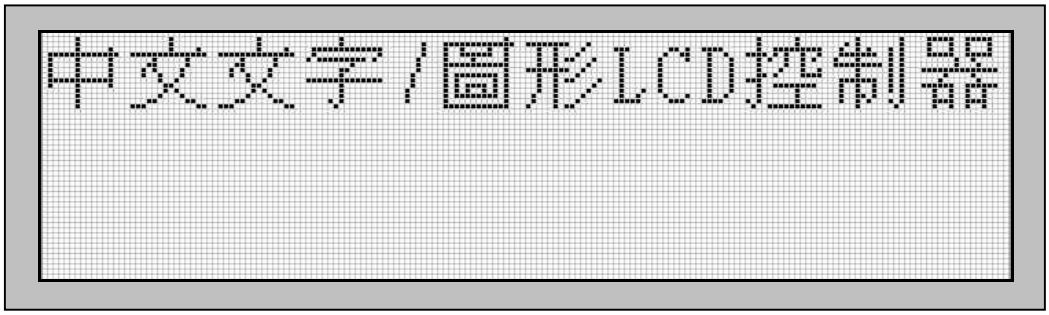

Figure 7-2: Mixed Display Mode of Full and Half Size Font

In the past, if user wants to show the Chinese character has to in the graphics mode and use bit map data to fill the Chinese font one byte by one byte. But the RA8803/8822 embedded hardware Chinese engine could accept two bytes Chinese BIG5 or GB code from MPU and show the character in text mode directly. Before the MPU pass 2bytes Chinese code to RA8803/8822, the user need to assign the cursor to the right position like traditional text mode. Because each Chinese code is 2byte, so if the MPU interface is use 8-bit then the MPU has to send twice(High byte and Low byte). If want to show English or numeric then MPU only need to send one byte ASCII code.

The RA8803 supports maximum 320x240 pixel resolution of display. Therefore the maximum full size character number at one page is 20x15, and half size character is 40x15. The RA8822 supports maximum 240x160 pixel display. Therefore the maximum full size character number at one page is 15x10, and half size character is 30x10.

7-1-1 Bold and Inverse

The RA8803/8822 also support the Bold and Inverse font. The user only needs to set up the related register bit that before send the character code to RA8803/8822.

7-1-2 Line Distance

The RA8803/8822 provide line distance feature. Especially in Chinese display, if add some space in each line will look better. The range of line distance is 1~16 pixel. Once the line distance is setup, the cursor will automatically move to property position for each line.

7-2 Chinese/English Text Alignment

Because the width of Chinese and English character is different, so if want to show text that include both character, it will meet “Alignment” problem. The RA8803/8822 provide a control bit to solve this problem.

1. Set REG. WCCR, Bit6 ALG = 1
2. Write “中文文字/圖形 LCD 控制器” twice, the display will show ”中文文字/圖形 LCD 控制器” ← The two text lines are aligning.

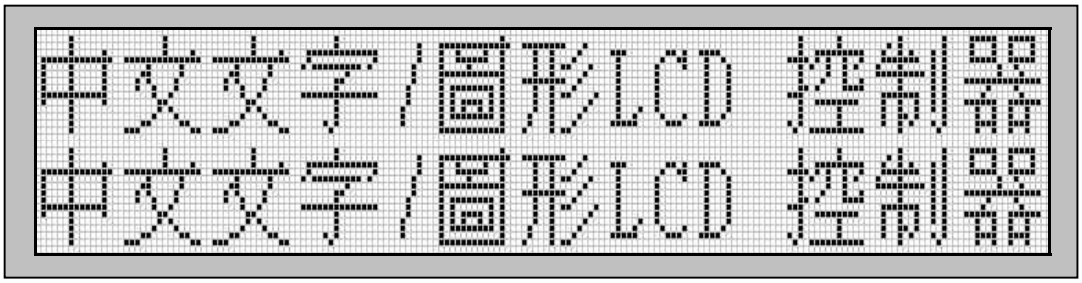

Figure 7-3: Text Align Example 1

1. Setup REG. WCCR, ALG = 1. Write “中文文字/圖形 LCD 控制器”
2. Setup REG. WCCR, ALG = 0. Write “中文文字/圖形 LCD 控制器” ← The two text lines are Non-align.

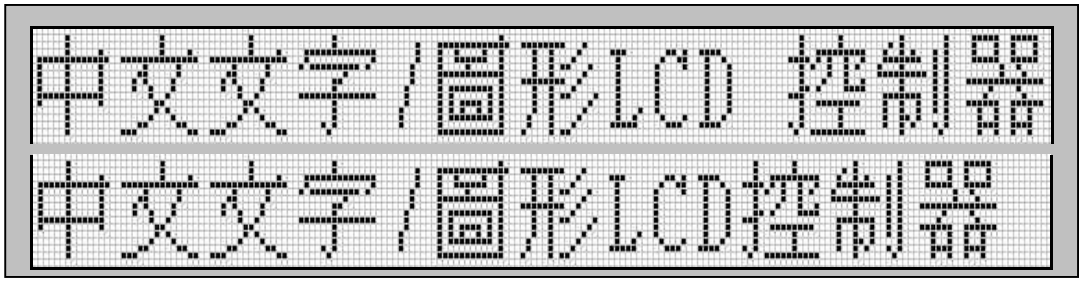

Figure 7-4: Text Align Example 2

7-3 Graphics Mode

The RA8803/8822 graphics mode is use bit map to fill the data on the Display RAM. The Figure 7-5 is an example to show how to set graphics mode.

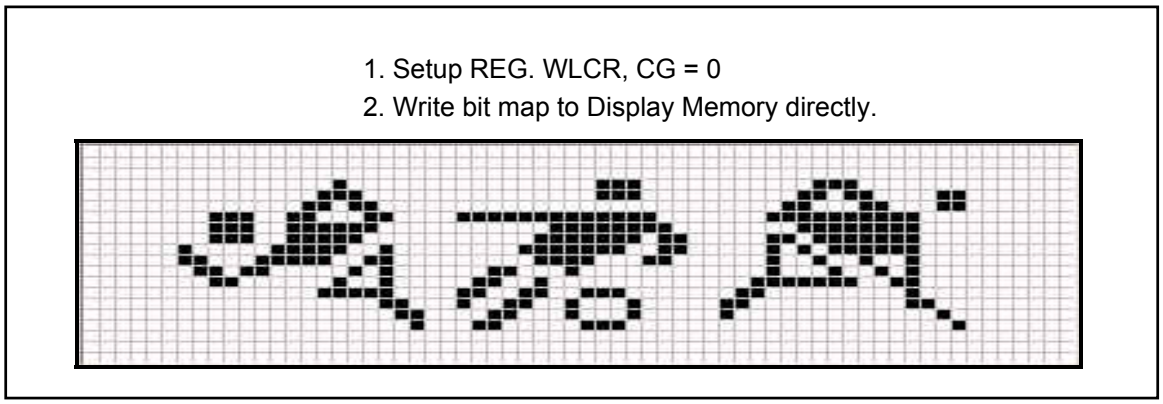

Figure 7-5: Graphics Mode

The RA8803 support maximum resolution is 320x240 pixel, therefore it need 9.6Kbyte(320x240/8 = 9600) Display Data RAM(DDRAM) to store each pixel data. The RA8822 support maximum resolution is 240x160 pixel, therefore it need 4.8Kbyte Display Data RAM. Figure 7-6 is an example to show the DDRAM data mapping to the LCD panel.

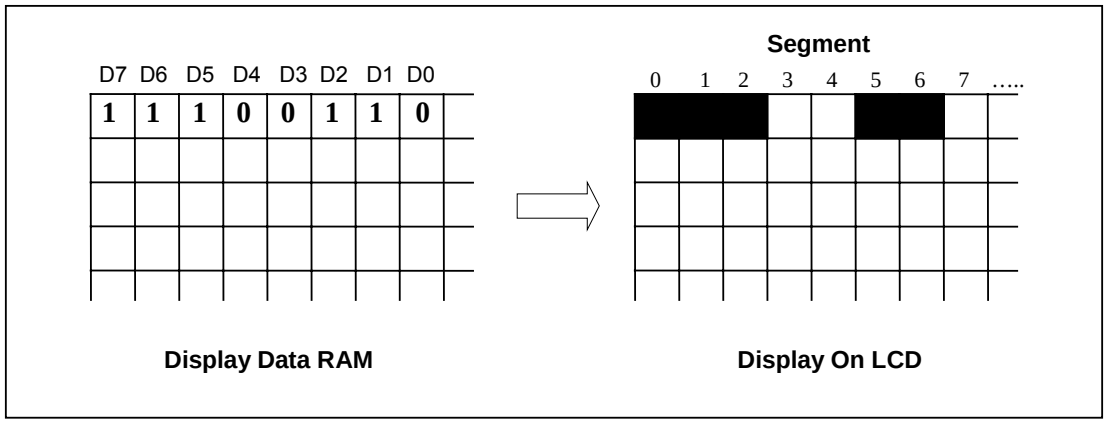

Figure 7-6: The Mapping of Display Data to LCD Panel

The RA8803/8822 provide an Auto-Write feature to fill a data to all of the DDRAM. At first, user write the data to Register PNTR then initial the Auto-Write function(Register FNCR Bit3). RA8803/8822 will fill the data to DDRAM in very short time. Normally this feature is used to clear screen or want to fill fixed pattern or background on screen.

7-4 Blinking and Inverse

The RA8803/8822 provide whole screen blinking or inverse function. Please refer to the control register - WLCR at chapter 5-2.

7-5 Cursor

7-5-1 Cursor Position and Shift

The cursor-moving unit of segment is one byte(or eight pixel). But the moving unit of common is one pixel. For example, if user want to show "制" at third location of upper-left, then the Register value are CPXR = 04h, CPYR = 00h. If user want to show "器" at first position of second line, the register value are CPXR = 00h, CPYR = 10h. Please refer to Figure 7-7.

The cursor position is controlled by Register CPXR and CPYR for both text and graphics mode. You can also setup the Auto-Increase mode for write to DDRAM or read data DDRAM. The cursor-moving boundary depends on the active window.

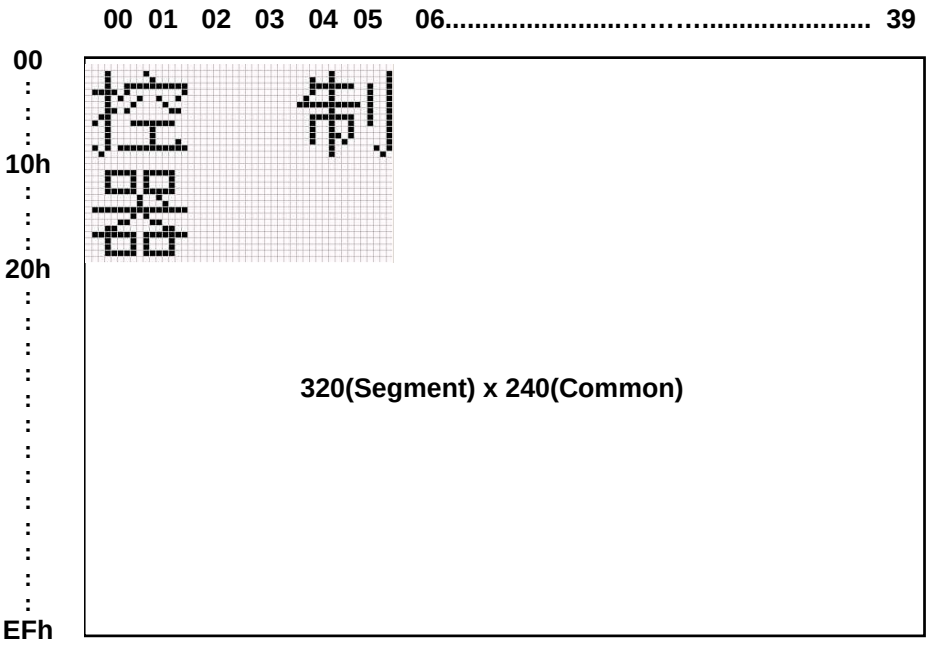

Figure 7-7: Example of RA8803 Cursor Position

7-5-2 Cursor Display and Blinking

The user could control cursor On/Off or Blinking. The register [80h] BTMR is used to set up the blinking time.

- Blinking Time = BTMR[80h] Bit[7..0] x (1/Frame_Rate)

7-5-3 Cursor Width and Height

The cursor height is controlled by register DWLR Bit[7..4], and the height is setting from 1~16pixel. It does depend on user's requirement.

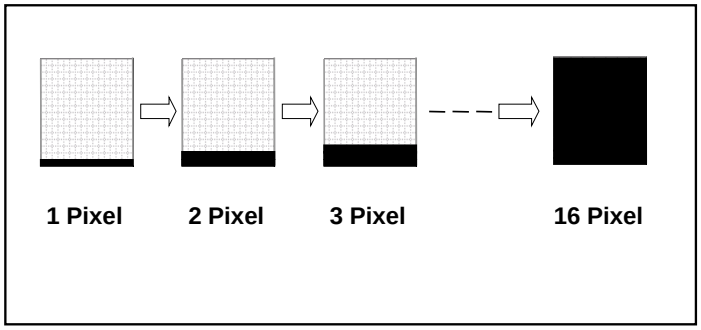

Figure 7-8: Cursor Height

In text mode, RA8803/8822 provide two widths for selection. If Register WCCR bit0 -- CSD = 0, the cursor width fixed to one byte(8 pixel). If CSD =1, the cursor width is depend on the previous character. If user sends a full size Chinese character, then the cursor width will become 2byte width(16 pixel). If user shows a half size character then the cursor width will change to one byte(8 pixel).

7-6 Display Window and Active Window

The RA8803/8822 provides two windows for real application -- Display Window and Active Window. The Display Window is the actual resolution of LCD panel. Active is a sub-window in Display Window. The boundary of cursor shift depends on the active window.

For RA8803, if LCD panel resolution is 320x240 pixel then the display window size is 320x240. We can create an active window in the display window like Figure 7-9. This figure show the display size is 320x240, and a 160x160 active window is on the upper-middle.

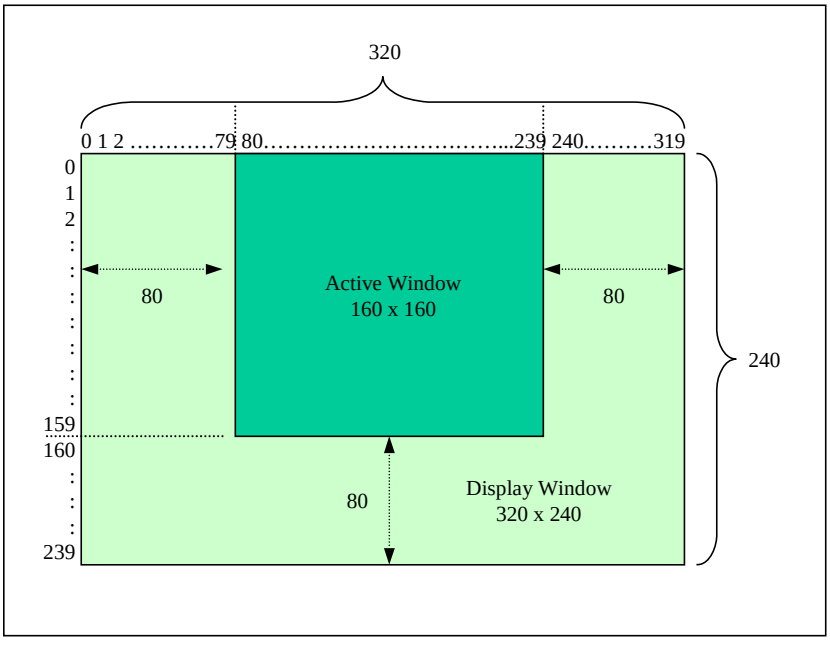

Figure 7-9: RA8803 Display Window and Active Window

For RA8822, if LCD resolution is 240x160 pixel then the display window size is 240x160. We can create an active window in the display window like Figure 7-10. This figure show the display size is 240x160, and a 120x120 active window is on the upper-left.

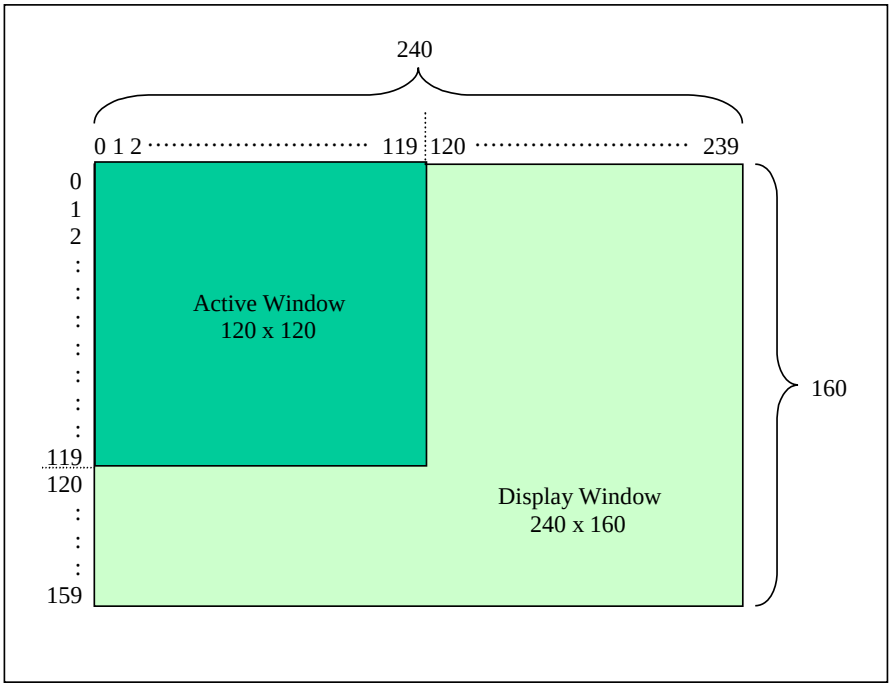

Figure 7-10: RA8822 Display Window and Active window

7-7 Two Layer Display

The RA8803/8822 embedded two DDRAM for two layers display. The Register MAMR is used to show the visible display for page1(layer1) and page2(layer2). It provide six display modes:

1. Display Page1
2. Display Page2
3. Display Page1 OR Page2
4. Display Page1 XOR Page2
5. Display Page1 NOR Page2
6. Display Page1 AND Page2

Please refer Figure 7-11 and Register description of MAMR Bit[6..4] and Bit[3..2].

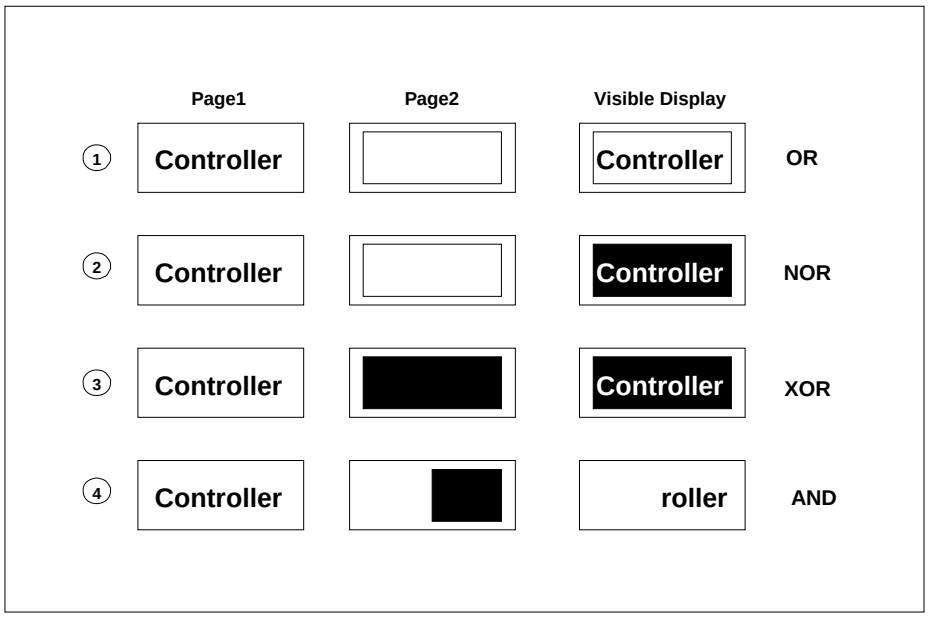

Figure 7-11: Two Layers Display

7-8 Horizontal Scrolling

The RA8803/8822 provide Horizontal Scrolling function. You can assign an area by Register BGCM and EDCM. Once start the horizontal scrolling, the assigned area will shift step by step and each step is 8-pixel width. The Figure 7-12 is an example for horizontal scrolling.

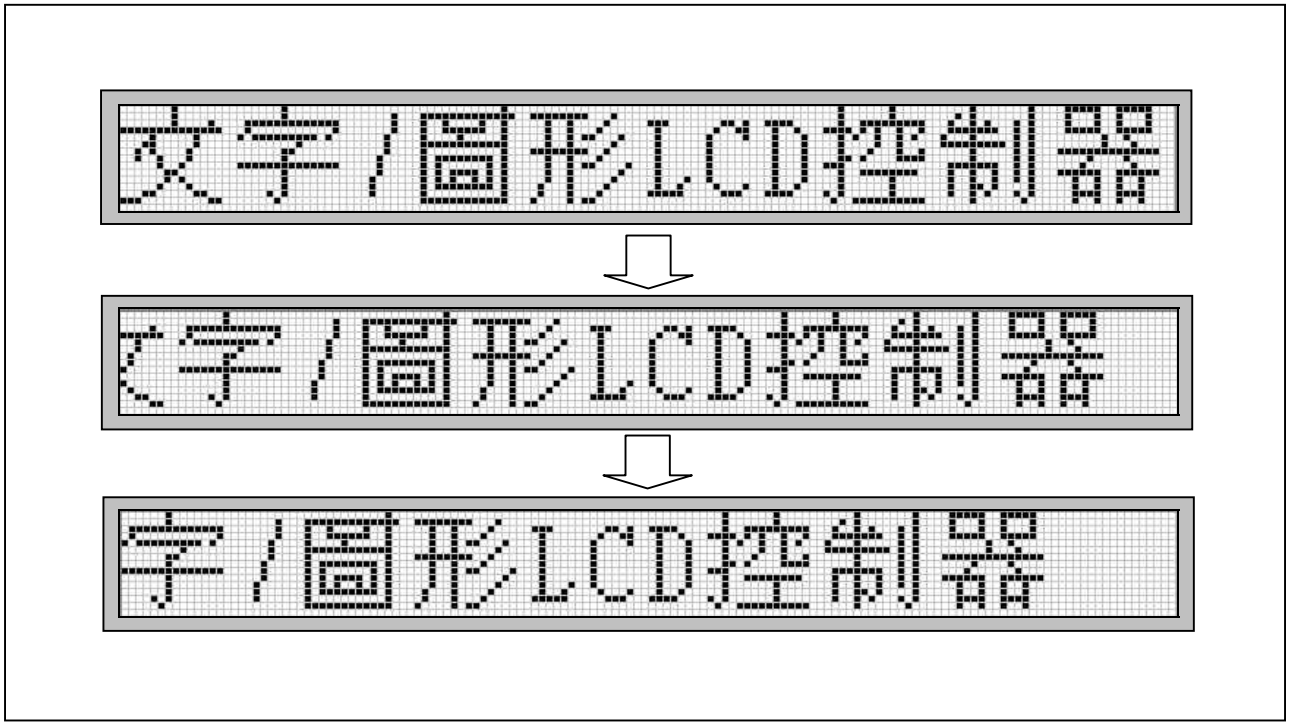

Figure 7-12: Horizontal Scrolling

7-9 Vertical Scrolling

The RA8803/8822 also provide Vertical Scrolling function. You can start the scrolling by control Register ADSR Bit2. Once start the vertical scrolling, the whole screen will shift step by step and each step is 1-pixel height. The Figure 7-13 is an example for vertical scrolling.

Figure 7-13: Vertical Scrolling

7-10 Gray Display

The RA8803/8822 also provide 4 level gray display. It used time-sharing to show the data in page1 and page2. The gray level of each pixel depends on the value of page1 and page2. For the same position,

the value of [page1, page2] could be [0,0], [1,0], [0,1] or [1,1]. Therefore if the display times are different then you will see the different gray level. Of course you have to speed up the display frame rate and system clock to get more good quality and to avoid screen flash.

7-11 Extension Mode for Display

RA8803/8822 support a special display mode – Extension mode. The dual page – page1 and page2 are show on the bigger panel. This mode is set by the Bit[6:4] of register MAMR. Please refer to Figure 7-14 and 7-15.

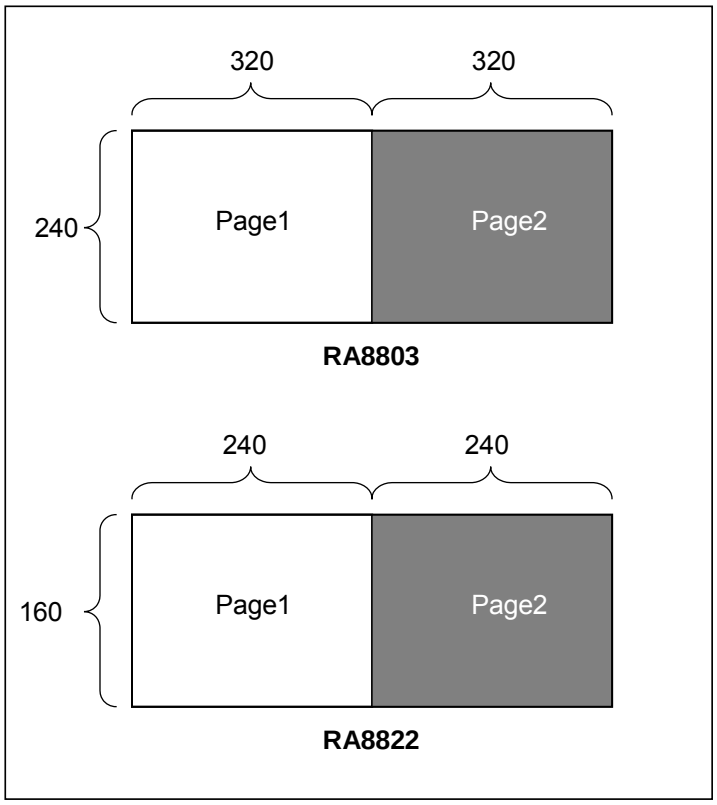

Figure 7-14：Extension Mode(1) Register MAMR bit[6:4] = 110h

If MAMR Bit[6:4]=110b, then RA8803 supports maximum resolution is 640x240 dots and RA8822 is 480x160. The left side of screen shows the Page1 of DDRAM, the right side shows the Page2. Please refer to Figure 7-14.

If MAMR Bit[6:4]=111b, then RA8803 supports maximum resolution is 320x480 dots and RA8822 is 240x320. The up side of screen shows the Page1 of DDRAM, the down side shows the Page2. Please refer to Figure 7-15.

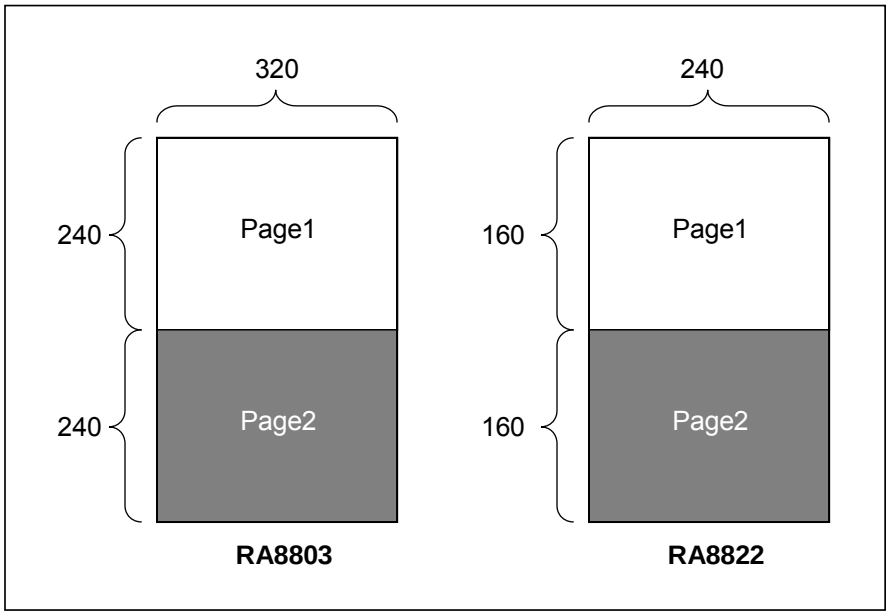

Figure 7-15：Extension Mode(2) Register MAMR bit[6:4] = 111h

8. Pin Assignment

8-1 Bonding Pad

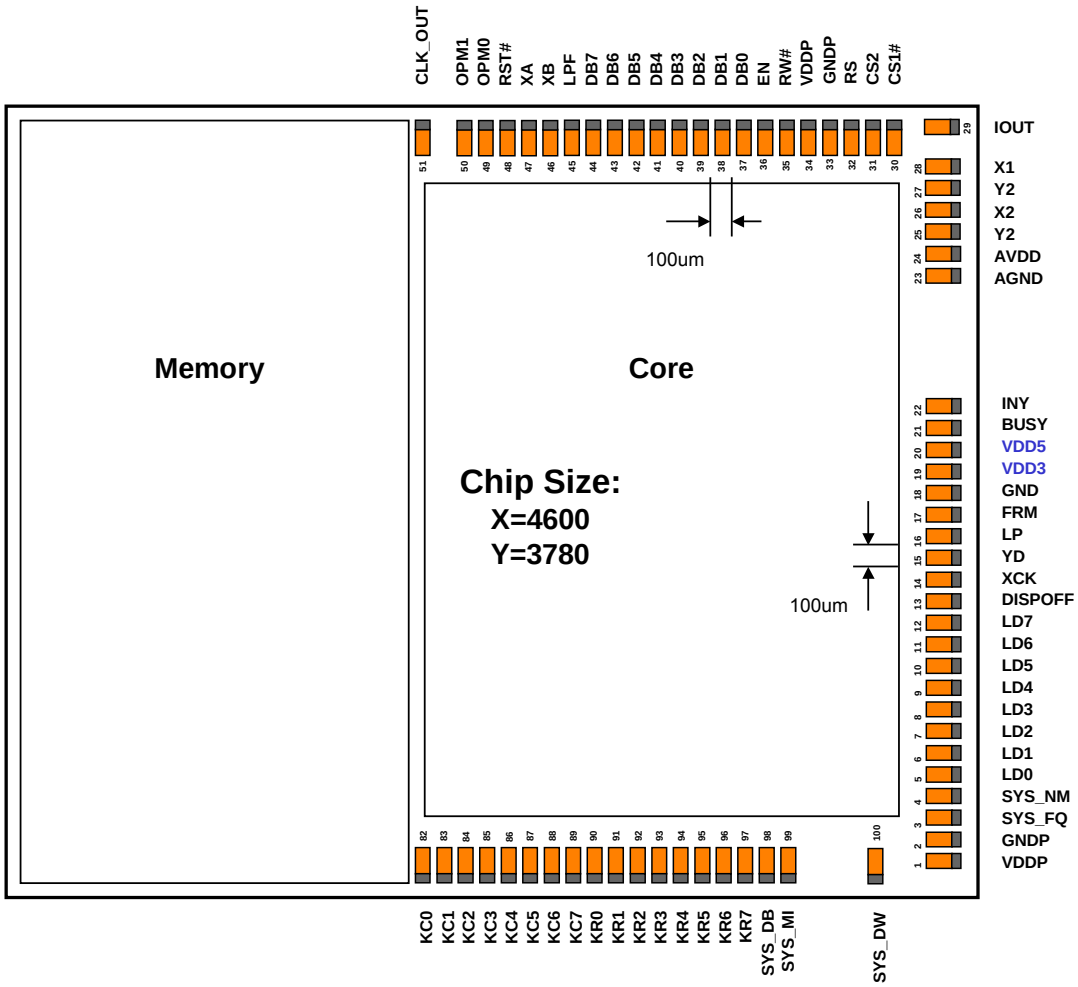

Figure 8-1: RA8803/8822 Bonding Pad

Note:

1. The Pad52~Pad81 are NC pins.
2. Chip Size is 4600 x 3780.
3. Most of the PAD Pitch are 100um.
4. The Bonding Window is 85um x 85um.
5. The chip size and X/Y Coordinate of RA8803 and RA8822 are same. But the internal memory architecture is different.

8-2 Pad X/Y Coordinate

Pad No.	Pad Name	X	Y
1	VDDP	2206.3	-1735.15
2	GNDP	2206.3	-1635.15
3	SYS_FQ	2206.3	-1535.15
4	SYS_NM	2206.3	-1435.15
5	LD0	2206.3	-1335.15
6	LD1	2206.3	-1235.15
7	LD2	2206.3	-1135.15
8	LD3	2206.3	-1035.15
9	LD4	2206.3	-935.15
10	LD5	2206.3	-835.15
11	LD6	2206.3	-735.15
12	LD7	2206.3	-635.15
13	DISPOFF	2206.3	-535.15
14	XCK	2206.3	-435.15
15	YD	2206.3	-335.15
16	LP	2206.3	-235.15
17	FRM	2206.3	-135.15
18	GND	2206.3	-35.15
19	VDD3	2206.3	64.85
20	VDD5	2206.3	164.85
21	BUSY	2206.3	264.85
22	INT	2206.3	364.85
23	AGND	2206.3	1015.34
24	AVDD	2206.3	1115.34
25	Y2	2206.3	1220.84
26	X2	2206.3	1327.84
27	Y1	2206.3	1433.83
28	X1	2206.3	1540.83
29	IOUT	2201.8	1795.98
30	CS1#	2001.8	1795.98
31	CS2	1901.8	1795.98
32	RS	1801.8	1795.98
33	GNDP	1701.8	1795.98
34	VDDP	1601.8	1795.98
35	RW#	1501.8	1795.98

Pad No.	Pad Name	X	Y
36	EN	1401.8	1795.98
37	DB0	1301.8	1795.98
38	DB1	1201.8	1795.98
39	DB2	1101.8	1795.98
40	DB3	1001.8	1795.98
41	DB4	901.8	1795.98
42	DB5	801.8	1795.98
43	DB6	701.8	1795.98
44	DB7	601.8	1795.98
45	LPF	490.55	1795.98
46	XB	381.3	1795.98
47	XA	272.05	1795.98
48	RST#	160.8	1795.98
49	OPM0	60.8	1795.98
50	OPM1	-39.2	1795.98
51	CLK_OUT	-231.2	1795.98
82	KC0	-322.55	-1795.99
83	KC1	-222.55	-1795.99
84	KC2	-122.55	-1795.99
85	KC3	-22.55	-1795.99
86	KC4	77.45	-1795.99
87	KC5	177.45	-1795.99
88	KC6	277.45	-1795.99
89	KC7	377.45	-1795.99
90	KR0	477.45	-1795.99
91	KR1	577.45	-1795.99
92	KR2	677.45	-1795.99
93	KR3	777.45	-1795.99
94	KR4	877.45	-1795.99
95	KR5	977.45	-1795.99
96	KR6	1077.45	-1795.99
97	KR7	1177.45	-1795.99
98	SYS_DB	1277.45	-1795.99
99	SYS_MI	1377.45	-1795.99
100	SYS_DW	1867.85	-1795.99

8-3 Pin Assignment

8-3-1 PQFP-100Pin

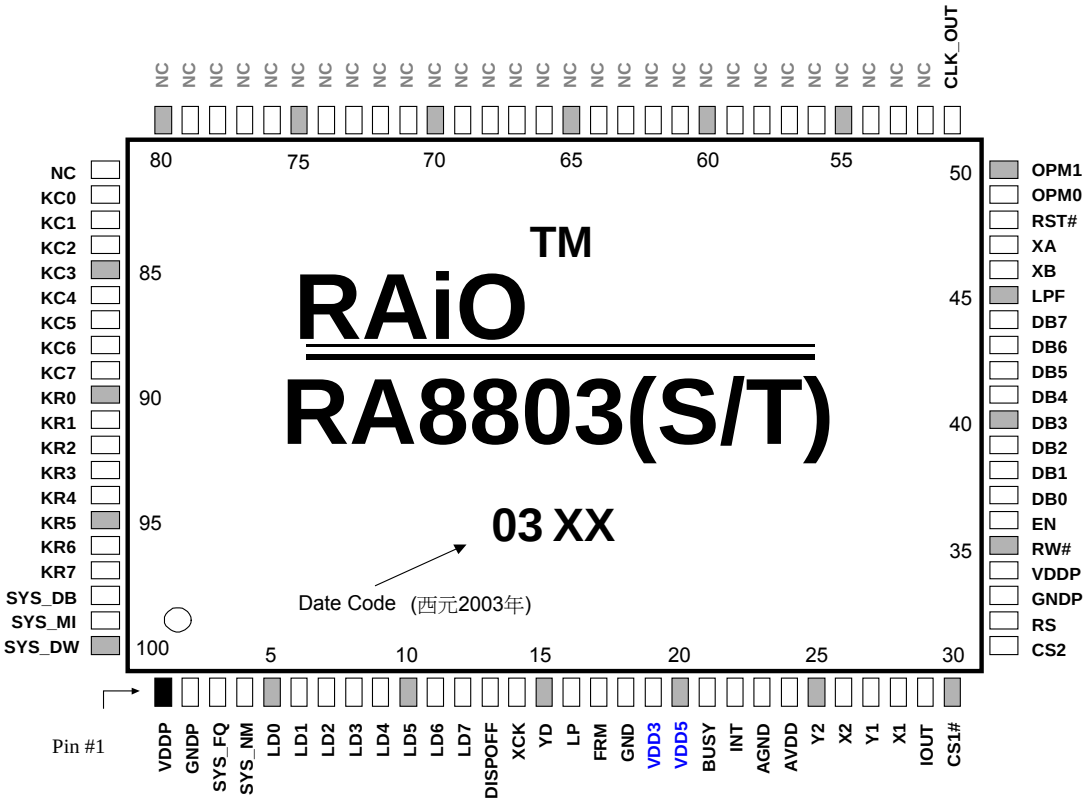

Figure 8-2: PQFP-100Pin Pin Assignment

RA8803/8822-S: Font ROM is Simple Chinese.

RA8803/8822-T: Font ROM is Traditional Chinese.

8-3-2 LQFP-100Pin(Body Size:14x20 mm)

The pin assignment is same as PQFP-100Pin.

8-4 RA8803/8822 Package Dimension

8-4-1 PQFP-100 Pin

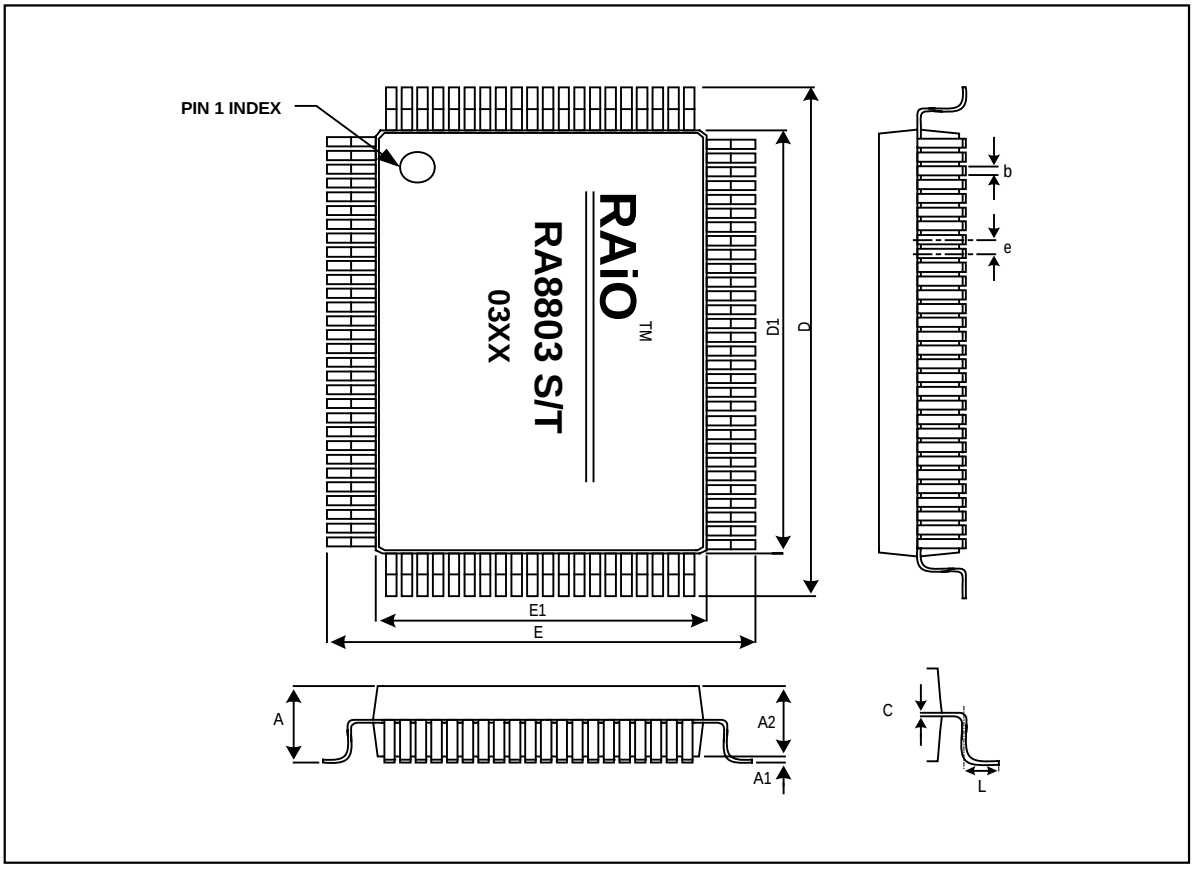

Figure 8-3：PQFP-100Pin Mechanical

Table 8-1

Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	--	--	3.40	--	--	0.134
A1	0.25	--	--	0.010	--	--
A2	2.54	2.79	3.05	0.100	0.110	0.120
b	0.23	--	0.38	0.009	--	0.015
C	0.13	0.15	0.20	0.005	0.006	0.008
E	16.94	17.20	17.45	0.667	0.667	0.687
E1	13.89	13.99	14.10	0.547	0.551	0.555
D	22.96	23.22	23.44	0.904	0.914	0.923
D1	19.89	19.99	20.09	0.783	0.787	0.791
e	--	0.65	--	--	0.0256	--
L	0.66	0.79	0.94	0.026	0.031	0.037

8-4-2 LQFP-100 Pin(Body Size:14x20 mm)

Table 8-2

Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	--	--	1.60	--	--	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09	--	0.20	0.004	--	0.008
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
e	--	0.65	--	--	0.026	--
L	0.45	0.60	0.75	0.018	0.024	0.030

8-5 Product Number

Product Name (Full Name)	Resolution (Max)	Package	Font ROM	RoHs Compliance
RA8803P1N-T	320x240	QFP-100 (14x20)	Traditional Chinese	Yes
RA8803P1N-S			Simple Chinese	Yes
RA8803P1-S			Simple Chinese	No
RA8803L2N-T		LQFP-100 (14x20)	Traditional Chinese	Yes
RA8803B-T		Die	Traditional Chinese	Yes
RA8803B-S			Simple Chinese	Yes
RA8822P1N-T	240x160	QFP-100 (14x20)	Traditional Chinese	Yes
RA8822P1N-S			Simple Chinese	Yes
RA8822P1-S			Simple Chinese	No
RA8822B-T		Die	Traditional Chinese	Yes
RA8822B-S			Simple Chinese	Yes

9. Electrical Characteristic

9-1 Absolute Maximum Ratings

Table 9-1

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V_{DD}	-0.3 to 6.5	V
Input Voltage Range	V_{IN}	-0.3 to V_{DD}+0.3	V
Operation Temperature Range	T_{OPR}	-20 to 80	℃
Storage Temperature	T_{ST}	-45 to 125	℃

9-2 DC Characteristic

Table 9-2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.3/5.0	5.5	V	
Input High Voltage	V_{IH}	0.8×V_{DD}	--	V_{DD}	V	
Input Low Voltage	V_{IL}	Gnd	--	0.2×V_{DD}	V	
Output High Voltage	V_{OH}	0.8×V_{DD}	--	V_{DD}	V	
Output Low Voltage	V_{OL}	Gnd	--	0.2×V_{DD}	V	
Input Leakage Current 1	I_{IH}	--	--	+1	μA	
Input Leakage Current 2	I_{IL}	--	--	-1	μA	
Standby Mode Current (Normal Mode Current)	I_{SB}	--	1.5	1.8	mA	Case1
			1.8	2.1	mA	Case2
Display Off Current	$I_{DISPLAY}$	--	120	140	μA	Case1
			140	160	μA	Case2
Off Mode	I_{OFF}	--	0.2	1	μA	Case1
		--	20	25	μA	Case2

Case1: V_{DDP} = V_{DD3} = A_{VDD} = 3.3V, V_{DD5} = NC, LCD Driver VDD = 5V, CLK = 4MHz, CLK_OUT: OFF, Segment=160, Common=160, FRM = 78Hz, T_A=25℃.

Case2: V_{DDP} = V_{DD5} = 5V, V_{DD3} = A_{VDD} = 3.3V, LCD Driver VDD = 3V, CLK = 4MHz, CLK_OUT: OFF, Segment=160, Common=160, FRM = 78Hz, T_A=25℃.